

1 CLAIMS

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3 1. A semiconductor device comprising:

4 a drain region having a first conductivity type;

5 a body region formed above said drain region
6 having a second conductivity type opposite said first
7 conductivity type;

8 a source region of said first conductivity type
9 formed in said body region so that said source region
10 is separated from said drain region by said body
11 regions;

12 an upward opening dielectric region lining a first
13 upward opening rectangular groove extending downward
14 through said source and said body regions and into said
15 drain region so that a first portion of said source
16 region and a first portion of said body region lie on
17 one side of said rectangular groove and a second
18 portion of said source region and a second portion of
19 said body region lie on the other side of said
20 rectangular groove, said upward opening dielectric
21 region defining a second upward opening rectangular
22 groove;

23 a gate region having a top surface, said gate
24 region completely filling the bottom portion of said
25 second upward opening rectangular groove, said top
26 surface of said gate region being situated between said
27 first portion and said second portion of said source
28 region; and

29 an insulating region having a planar top surface
30 formed above said gate region and above said first and
31 said second portions of said source and said body
32 regions.

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34 2. A semiconductor device as in Claim 1 wherein said
35 source and said body regions are formed in an epitaxial
36 layer having said first conductivity type.

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38 3. A semiconductor device as in Claim 1 wherein said

1 drain region comprises a semiconductor substrate, said body
2 region consists of an epitaxial layer formed on said
3 substrate, and said gate region extends into said
4 substrate.

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6 4. A semiconductor device as in Claim 1 wherein said
7 drain region comprises a semiconductor substrate and a
8 selected portion of an epitaxial layer formed on said
9 semiconductor substrate and said gate region extends through
10 said epitaxial portion of said drain region into said
11 substrate.

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13 5. A semiconductor device as in Claim 1 further
14 including a fourth region having said second conductivity
15 type, said fourth region underlying said drain region, said
16 first portion of said body region, said drain region, and
17 said fourth region comprising an emitter, base, and
18 collector, respectively, of a junction transistor.

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20 6. A semiconductor device comprising:

21 a block of semiconductor material having a top
22 surface;

23 an upward opening dielectric region lining an
24 upward opening rectangular groove extending downward
25 from said top surface into said block of semiconductor
26 material, said upward opening dielectric region thereby
27 defining a second upward opening rectangular groove;

28 a source region of first conductivity type
29 extending downward into said block of semiconductor
30 material from said top surface adjacent a first portion
31 of said dielectric region;

32 a body region of second conductivity type opposite
33 said first conductivity type in said block of
34 semiconductor material, said body region underlying and
35 being adjacent said source region and being adjacent a
36 second portion of said dielectric region;

37 a drain region of said first conductivity type in
38 said block of semiconductor material, said drain region

1 being adjacent and underlying said body region and
2 being adjacent a third portion of said dielectric
3 region;

4 a gate region having a top surface, said gate
5 region completely filling the bottom portion of said
6 second upward opening rectangular groove, said top
7 surface of said gate region being opposite said source
8 region; and

9 an insulating material having a planar top surface
10 formed above said gate region and above said source
11 region.

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13 7. A semiconductor device as in Claim 6 further
14 comprising a region of said second conductivity type
15 underlying said drain region, wherein

16 a portion of said body region, a portion of said
17 drain region and a portion of said region of said
18 second conductivity type underlying said drain region
19 comprise a junction transistor.

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21 8. A method of making a semiconductor device
22 comprising the following steps:

23 forming a first region of a semiconductor material
24 having a first conductivity type;

25 forming a second region of a semiconductor
26 material having a second conductivity type above and in
27 contact with said first region, said second region
28 having a top surface;

29 forming a third region of said first conductivity
30 type in a first portion of said second region, said
31 third region extending to a first portion of said top
32 surface;

33 forming a first rectangular groove in said first
34 portion of said top surface, said rectangular groove
35 extending downward through said third and said second
36 regions into said first region so that a first portion
37 of said third region and a first portion of said second
38 region lie on one side of said rectangular groove and a

1 second portion of said third region and a second
2 portion of said second region lie on the other side of
3 said rectangular groove;

4 lining said ^{first} rectangular groove with a dielectric
5 material thereby forming a second, inner rectangular
6 groove;

7 filling the bottom portion of said second, inner
8 rectangular groove with a conductive material so that a
9 top surface of said conductive material in said second
10 groove lies between said first portion and said second
11 portion of said third region;

12 forming an insulating layer having a planar top
13 surface over the device resulting from the preceding
14 steps.

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16 ²/₈. A method as in Claim ¹/₈ wherein said first region
17 is formed on a fourth region of semiconductor material of
18 said second conductivity type.

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20 ^{Sub B3} 10. A method of making a semiconductor device
comprising the following steps:

21 forming a first region of a semiconductor material
22 having a first conductivity type;

23 forming a second region of a semiconductor
24 material having a second conductivity type above and in
25 contact with said first region, said second region
26 having a top surface;

27 forming a third region of said first conductivity
28 type in a first portion of said second region, said third
29 region extending to a first portion of said top surface;

30 forming a first rectangular groove in said top
31 surface, said groove extending downward into said first
32 region so that a portion of said third region and a
33 portion of said second region lies adjacent said groove
34 on one side of said groove;

35 lining said ^{first rectangular} groove with a dielectric material
36 thereby forming a second, inner rectangular groove;

37 filling the bottom portion of said second, inner
38

1 rectangular groove with a conductive material so that a
2 *a* top surface of said conductive material in said second *inner*
3 groove lies opposite said portion of said third region;
4 forming an insulating layer having a planar top
5 surface over the device resulting from the preceding
6 steps.

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8 *4* 11. A method as in Claim *3* wherein said first region
9 is formed on a fourth region of semiconductor material of
10 said second conductivity type.

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